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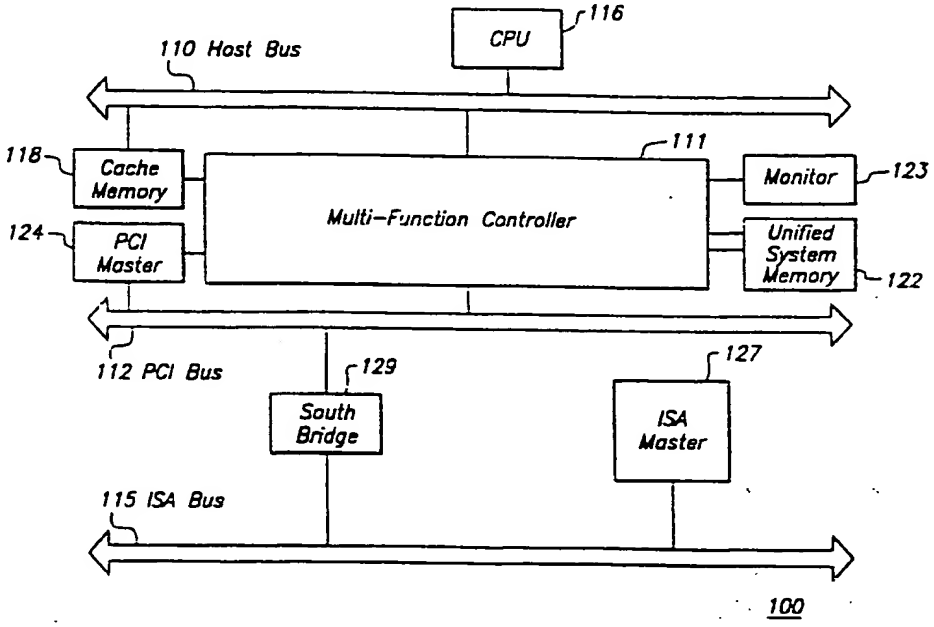
(54) Title: MULTI-FUNCTION CONTROLLER AND METHOD FOR A COMPUTER GRAPHICS DISPLAY SYSTEM



(57) Abstract

A multi-function controller (111) in a computer graphics system performs the functions of a graphics processor, a video processor, a system memory controller, a cache controller, and a PCI bridge. The multi-function controller (111) is connected to the host bus (110) of the computer graphics display system to maximize performance. A graphics frame buffer and a system memory are combined into a unified system memory (122), which is controlled by and coupled to the multi-function controller (111).

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MULTI-FUNCTION CONTROLLER AND METHOD FOR A COMPUTER GRAPHICS DISPLAY SYSTEM

Background of the Invention

1. Field of the Invention

This invention relates generally to a computer graphics/video display system, and more specifically to an multi-function controller in a computer graphics/video display system.

2. Description of the Related Art

Figure 1 illustrates a conventional computer graphics/video display system **10** that generates a graphics or video image. This system includes three buses: a host bus **22**, a Peripheral Component Interconnect/Interface (PCI) bus **24** and an Industry Standard Architecture (ISA) bus **26**. The host bus **22** can run at 50-100 MHz and can be 8 or more bytes wide. The PCI bus **24**, which is an industry standard bus, runs at 33 MHz and is 4 bytes wide, and the ISA bus **26**, which is also an industry standard bus, runs at 6-8 MHz and is two bytes wide.

A central processing unit (CPU) **28** and a cache memory **30** are connected to the host bus **22**. A cache controller/system memory controller/PCI bridge unit **32**, connected to both the host bus **22** and the PCI bus **24**, controls the cache **30** and a system memory device **34** and controls information flow between the host bus **22** and the PCI bus **24**. A data buffer **36**, connected to both the host bus **22** and the PCI bus **24**, stores data traveling to and from the memory device **34**. A PCI bus master **35** controls the transfer of information on the PCI bus **24** to and from the system memory **34**.

A south bridge **42**, which is connected between the ISA bus **26** and the PCI bus **24**, controls information traveling between the PCI bus **24** and the ISA bus **26**. An ISA bus master **44** controls the flow of information on the ISA bus **26** to and from the system memory **34**. In response to a command from the CPU **28**, a graphics processor **46** generates graphics data, which is then stored in a local frame buffer **47** or displayed as an image on a monitor **20**. In response to a command from the CPU **28**, a video processor **37** generates video data for display on monitor **20**.

A disadvantage with the system illustrated in Figure 1 is that the PCI bus **24**, to which the graphics and video processors are connected, does not have enough speed to allow the graphics and video processors to perform the functions required by many

advanced graphics/video display systems. Specifically, the graphics and video processors cannot access system memory 34 as quickly as is desired. Additionally, the system illustrated in Figure 1 does not give the graphics and video processors direct access to system memory 34, thus resulting in a higher cost because a local frame buffer 47 must be used. Therefore, there is a need for a graphics/video display system which will have a graphics/video processor that can easily access system memory, which will have the capacity to perform functions required by advanced graphics systems, and which will be economical.

Summary of the Invention

The present invention provides a method and a system for displaying graphics or video images on a monitor. Using a novel architecture, the present invention combines the above-described functions of the graphics processor, the video processor, and the system memory controller/cache controller/PCI bridge unit into an multi-function controller connected to both the host bus and the PCI bus (or other similar buses). The multi-function controller may comprise one or more chips.

By incorporating the graphics/video processor into a controller that is linked to the host bus, the present invention overcomes the conventional system limitations associated with coupling the graphics processor to the PCI bus. Since the host bus is faster than the PCI bus, information can travel faster to and from the graphics/video processor than it would travel if the graphics/video system were just coupled to the PCI bus.

Moreover, in one embodiment, the graphics frame buffer and the system memory are combined into a unified system memory, which is controlled by the multi-function controller. A unified system memory has more space than a regular frame buffer, and using the unified system memory uses less parts than using both a frame buffer and a separate system memory. Additionally, having the multi-function controller control the unified system memory allows the graphics/video processor to have direct access to the unified system memory.

In a preferred embodiment, the multi-function controller is divided into a combined PCI bridge/cache controller and a unified graphics/video controller. The combined PCI bridge/cache controller includes a PCI bridge and a cache controller. The unified graphics/video controller includes a graphics/video processor and a system memory controller. By integrating the PCI bridge and cache controller and by

integrating the graphics/video processor and the system memory controller, the number of chips in the system of the present invention is reduced.

The combined PCI bridge/cache controller and the unified graphics/video processor are coupled by a communications link. All commands for the unified graphics/video controller from various components in the system of the present invention are sent to the combined PCI bridge/cache controller, which via the communications link, passes the commands to the unified graphics/video controller. Sending all commands for the unified graphics/video controller to the combined PCI bridge/cache controller promotes efficiency because commands are then directly sent to the unified graphics/video controller from only one place.

Brief Description of the Drawings

Figure 1 is a block diagram of a conventional graphics/video display system.

Figure 2 is a block diagram of a preferred embodiment for a computer graphics display system, including the multi-function controller, according to the present invention.

Figure 3 is a block diagram of the computer graphics display system showing the multi-function controller in more detail.

Figure 4 is a block diagram of a preferred embodiment of a unified graphics/video controller located within the multi-function controller according to the present invention.

Figure 5 is a block diagram of data buffers and data path within the unified graphics/video controller of the present invention.

Figure 6 is a block diagram of a combined PCI bridge/cache controller located within the multi-function controller of the present invention.

Figure 7 is a flow chart illustrating the communication flow between the unified graphics/video controller and combined PCI bridge/cache controller.

Detailed Description of the Preferred Embodiment

Figure 2 illustrates a preferred embodiment of the computer graphics display system 100 of the present invention. The system 100 includes three main buses: a host bus 110, a Peripheral Component Interconnect/Interface (PCI) bus 112 and an Industry

Standard Architecture (ISA) bus **115**. The host bus **110** preferably runs at 50-100 MHz and is eight or more bytes wide. The PCI bus **112** runs at approximately 33 Mhz and is four bytes wide and the ISA bus **115** runs at 6-8 Mhz and is two bytes wide. A central processing unit (CPU) **116**, such as the Intel Pentium Processor, is connected to the host bus **110**.

Coupled to both the host and PCI buses **110**, **112** is a multi-function controller **111**. The multi-function controller **111** performs the functions of a PCI bridge, cache controller, system memory controller, and graphics/video processor. In an alternate embodiment, the multi-function controller **111** may incorporate other components such as an audio processor (not shown) and other multimedia components (not shown).

A unified system memory **122**, which stores both system and graphics/video data, and a cache memory **118** are coupled to the multi-function controller **111** and controlled by the multi-function controller **111**. A monitor **123** displays graphics or video images generated by the multi-function controller **111**. For instance, the monitor **123** could be a conventional CRT or LED panel.

A PCI bus master **124** controls the transfer of information on the PCI bus to and from the system memory **122**, and an ISA bus master **127** controls the transfer of information on the ISA bus. A south Bridge **129** couples the ISA and PCI buses and controls information traveling between the PCI and ISA buses **112**, **115**.

The unified system memory device **122** includes a section for graphics and video data and a section for data for the rest of the system **100**. An example of the system memory device **122** is one that includes up to five sixty-four bit banks, where each bank consists of two conventional thirty-two bit single in-line memory modules (SIMM) or one conventional sixty four bit dual in-line memory module (DIMM). This allows for a range of from four to 512 megabytes of system memory, where from .5 megabytes to four megabytes of system memory are dedicated to graphics data.

Referring to Figure **3**, the multi-function controller **111** is shown in detail and comprises a combined PCI bridge and cache controller **114**, a communications link **126**, and a unified graphics/video controller **120**. The multi-function controller **111** can be a single chip or several chips, and, in one embodiment, all the components of the combined PCI bridge/cache controller are integrated into one chip and all the components of the unified graphics/video controller are integrated into another chip.

The unified graphics/video controller **120** has four principal functions: (1) generating graphics or video information in response to a command from the CPU **116**,

(2) controlling the unified system memory device 122, (3) temporarily storing and routing data traveling to and from either the CPU 116, the cache 118, the system memory device 122 or a graphics/video processor within the unified graphics/video controller 120, and (4) generating the graphics/video image on the monitor 123.

The combined PCI bridge/cache controller unit 114 has four principle functions: (1) controlling the cache 118, (2) controlling information traveling between the PCI bus 112 and the host bus 110, (3) controlling access to the PCI bus, and (4) conveying to the unified graphics/video controller 120 information from either the CPU 116 or a PCI bus master 124, as well as from either the cache 118 or the ISA or PCI buses 112, 115.

The communications link 126 connects the unified graphics/video controller 120 and the combined PCI bridge/cache controller 114. The communications link 126 transfers data, address and control information between the unified graphics/video controller 120 and the combined PCI bridge/cache controller 114. The communications link 126 provides an information path that is preferably equal or wider that the width of the PCI bus 112 and that is preferably the same speed or faster than the PCI bus 112. In one embodiment, the communications link 126 is a time multiplexed, synchronous bus that has half the width and twice the speed of the PCI bus 112 and that uses nine lines to carry handshaking signals and twenty lines to carry data, control and address information.

A CPU-control bus 130 carries address and control information to and from the CPU 116 and the combined PCI bridge/cache controller unit 114. Similarly, a PCI-control bus 132 carries address, control, and data information between the combined PCI bridge/cache controller unit 114 and the PCI bus master 124. A CPU-data bus 134 carries data between the CPU 116 and the unified graphics/video controller 120, and a monitor bus 135 carries information from the unified graphics/video controller 120 to the monitor 123. Additionally, control and address signals travel between the unified graphics/video controller 120 and the unified system memory device 122 along a memory-control bus 136, and data travels between the unified graphics/video controller 120 and the unified system memory device 122 along a memory-data bus 138.

In one embodiment, all control and address information for the unified graphics/video controller 120 from the CPU 116 is sent to the PCI bridge/cache controller 114, which, via the communications link 126, instructs the unified graphics/video controller 120 accordingly. For example, when the CPU 116 needs to write data to or read data from either the unified system memory device 122 or a buffer

in the unified graphics/video controller 120, the CPU 116 transmits the appropriate control and address information to the combined PCI bridge/cache controller 114 via the CPU-control bus 130. The combined PCI bridge/cache controller 114 then transmits the address and control information to the unified graphics/video controller 120 through the communications link 126.

If the command is a read, the unified graphics/video controller 120 passes the requested read data to the CPU 116 or the cache 118. Specifically, the unified graphics/video controller 120 retrieves the read data from a specified address and places it on the CPU-data bus 134 for sampling by the CPU 116 or the cache 118. The unified graphics controller 120 then informs the combined PCI bridge/cache controller, via the communications link 126, that the read command has been executed, and the combined PCI bridge/ cache controller 114 informs the CPU 116, via the cpu-control bus 130, that the read data is on the cpu-data bus 134.

If the command is a write, the unified graphics/video controller 120 retrieves the write data from the CPU 116 or the cache 118 and stores it. Specifically, the CPU 116 or the cache 118 drives the write data on the CPU-data bus 134, where the unified graphics/video controller 120 retrieves it. The write data is then stored within the unified graphics/video controller 120 or within the system memory device 122, depending on the address information sent by the CPU 116 via the combined cache controller/PCI bridge 114. The unified graphics/video controller 120 sends a signal, via the communications link 126, to the combined cache controller/PCI bridge 114 after it has retrieved the write data from the cpu-data bus 134. The combined PCI bridge/cache controller 114 then informs the CPU that the write data no longer need to be driven on the cpu-data bus 134.

Control and address information from the PCI bus master 124 to the unified graphics/video controller 120 also passes through the PCI bridge/cache controller 114. For instance, when the PCI bus master 124 needs to read data from or write data to the unified system memory device 122 or a buffer in the unified graphics/video controller 120, the PCI bus master 124 transmits the control, the address, and any data information to the combined cache controller/PCI bridge 114 via a PCI-control bus 132. The combined PCI bridge/cache controller 114 then conveys the control, address, and data information to the unified graphics/video controller 120.

If the command is a read, the unified graphics/video controller 120 sends the requested data through the PCI bridge/cache controller. Specifically, the unified

graphics/video controller 120 retrieves the read data from the location specified by the PCI master 124 and sends it to the combined cache controller/PCI bridge 114 via the communications link 126. The combined cache controller/PCI bridge 114 then drives the data on the PCI-control bus 132.

If the command is a write, the PCI bus master send the write data to the combined cache controller/PCI bridge 114 via the PCI-control bus 132. The combined cache controller/PCI bridge 114 then drives the data on the communications link 126, where the unified graphics/video controller 120 retrieves it. The write data is then stored within the unified graphics/video controller 120 or within the unified system memory device 122.

If the CPU 116 wants to read data from a register or memory connected to the PCI bus or ISA buses 112, 115, it will send the appropriate address and control information to the combined PCI bridge/cache controller 114, which will pass the information to the location designated in the address information. The CPU 116 will receive the requested read data through the unified graphics/video controller 120. In particular, the combined PCI bridge/cache controller 114 will retrieve the read data from the PCI bus 112 and send it to the unified graphics/video controller 120, which will then place the data on the CPU-data bus 134 for sampling by the CPU 116. When the CPU 116 needs to write data to a register or memory connected to the PCI or ISA bus 112, 115, it will send the appropriate command and address information via the CPU-control bus 130 to the combined cache controller/PCI bridge unit 114, which will then signal the unified graphics/video controller 120 to sample write data driven on the CPU-data bus 136 by the CPU 116. The unified graphics/video controller 120 will then send, via the communications link 126, the data to the combined cache controller/PCI bridge unit 114, where the data will be driven on the PCI-control bus 132 and sent to the appropriate component or agent on the PCI bus 132.

Referring now to Figure 4, there is shown a block diagram of the unified graphics/video controller 120. The unified graphics/video controller 120 interfaces with communications link 126 at a communication link interface 140 and with the host bus at a host interface 142. A graphics/video processor 144, such as any 3D graphics processor manufactured by S3, Inc. or such as any graphics processor from the Trio or Virge family of graphic/video processors (e.g. Trio 64V+) manufactured by S3, Inc., of Santa Clara, CA, generates graphics and video information in response to a command from the CPU 116. The CPU 116 sends commands to the graphics/video processor 144 by

writing data either directly to the graphics/video processor **144** or to the unified system memory **122**, where it is later retrieved by the graphics/video processor **144**. The unified graphics/video controller **120** also includes a system memory controller **146** for controlling the system memory device **122**. The integration of the system memory controller **146** into the unified graphics/video controller **120** provides tighter control and more flexibility in handling memory data access from various sources. The system memory controller **146** is created using known unified memory design techniques.

Information travels through the unified graphics/video controller **120** via an internal bus **148**. Note that, although Figure **4** illustrates the monitor **123** directly connected to the graphics/video processor **144**, the monitor **123** may be connected to the internal bus **148** instead (and thus coupled to the graphics/video processor through the internal bus **148**). Similarly, the unified system memory device **122** may be connected to the internal bus **148** instead of the system memory controller **146**.

Figure **5** illustrates an example of the layout of the data buffers used for the data path in the host interface **142**, the communications link interface **140**, the graphics/video processor **144**, and the system memory controller **146**. With respect to the host interface **142**, data from the CPU **116** may be stored in the I/O registers **210**. All data traveling to the host bus **110** passes through multiplexer **212** before being placed on the CPU-data bus **134**. Data from the cache **118** or the CPU **116** that is to be written into the system memory **122** travels through a 64x1 pipe register **218** to a multiplexer **220** and into a memory write buffer **216**, where, if necessary the data is temporarily stored before being written into the system memory **122**. A PCI write buffer **232** temporarily stores data from the CPU **116** and en route to the PCI bus **112** before the unified graphics/video controller **120** places the data on the communications link **126**. Similarly, the unified graphics/video controller **120** temporarily stores data traveling from the CPU **116** to the graphics processor **144** in a write buffer **226**. The write buffer **226** then passes the data to a multiplexer **228**, where it is subsequently transferred to the graphics processor **144**.

With respect to the communications link interface **140**, data traveling from the communications link **126** to the host bus **110** travels through a 64x2 pipe register **230**. Data to be stored in the graphics processor **144** or the system memory **122** passes through a 64x1 pipe register **246**. A queue controller **244** receives control signals from the combined PCI bridge/cache controller **114**, and from the control signals generates a select signal which controls a multiplexer **234**. The multiplexer **234** receives all data traveling to the communications link **126**. The select signal determines which data will

be passed to a dissembler 236, which divides the sixty-four bit data into a number of parts, depending on the width of the communications link. For instance, if the communications link 126 is sixteen bits wide, the data is divided into four sixteen bit parts. From the dissembler 236, the data then travels to a 16x1 pipe register 238 and on the communications link 126.

With respect to the memory controller 146, all data traveling to the system memory 122 passes through a multiplexer 222, and all data retrieved from the system memory 122 is temporarily stored in a memory prefetch buffer 214. Within the graphics processor 144, a command FIFO 224 stores graphics commands received from the CPU. Additionally, a graphics buffer 225 stores graphics data generated by the graphics processor 144 and traveling between the graphics processor 144 and the system memory 122.

Referring now to Figure 6, there is shown the combined PCI bridge/cache controller 114. At a communications link interface 260, the combined PCI bridge/cache controller unit 114 transmits address, control and data information to the unified graphics/video controller 120 in response to the combined PCI bridge/cache controller receiving a command for the unified graphics/video controller. Specifically, as shown in Figure 7, communications link interface 260 sends 710 a start signal to communications link interface 140 in the unified graphics video controller 120 indicating the start of communications link bus cycle. Communications link interface 260 then sends 720, via the communications link 126, the command and any corresponding address and data information to the communications link interface 140 via the communications link 126. The unified graphics/video controller 120 then performs 730 the task specified the command. After the task has been performed, communications link interface 140 sends 740 a done signal, via the communications link 126, to communications link interface 260, indicating that the command has been carried out and thereby ending the communications link 126 bus cycle.

In some cases, the communications link interface 140 may send the done signal one clock cycle before the unified graphics/video controller 120 completes execution of the command. For instance, if the command requires that the unified graphics/video controller 120 drive data requested by the CPU 116 on the cpu-data bus 134, one communications link 126 clock cycle before the unified graphics/video controller 120 drives the data on the cpu-data bus 126, communications link interface 140 will send the done signal to communications link interface 260. This is because by the time the

combined PCI bridge and cache controller **114** informs the CPU **126** that data is waiting on the cpu-data bus **134**, the unified graphics/video controller will have already driven the data on the cpu-data bus **134**. Communications link interfaces **260** and **140** are implemented using known interface design techniques.

At a host interface **262**, the combined PCI bridge/cache controller **114** transmits address, control, and data information to the CPU **116** and receives address, control, and data information from the CPU **116**. The host bus interface **262** determines where information received at the combined cache controller/PCI bridge **114** should be sent, and sends the information to the appropriate place (e.g. cache **118**, unified graphics/video controller **120**, PCI bridge **264**, and etc.). Information being sent from the PCI bridge/cache controller **114** to the host bus is sent out through the host interface **262**. The host interface **262** is implemented using known interface design techniques.

The combined PCI bridge/cache controller includes a conventional PCI bridge **264**, which controls information traveling between the host bus **110** and the PCI bus **112**, and includes a conventional cache controller **266**, which controls the transfer of data between the cache **118** and the host bus **110**. Information travels through the combined PCI bridge/cache controller **114** on an internal bus **268**.

The combined cache controller/PCI bridge **114** also includes a conventional bus arbiter **270** which controls access to the PCI bus **112**. Components of the graphics display system **100** that initiate use of the PCI bus **112** have a grant line and a request line coupled to the bus arbiter **270**. Each of such components is assigned a fixed priority for bus access. The bus arbiter **270** receives bus access requests on the request lines from different components on the PCI bus **112** and grants bus access to the requesting component with the highest priority by asserting a grant signal on the grant line coupled to that component.

CLAIMS

What is claimed is:

1. A controller for use in a computer graphics system having a system memory, the graphics processor comprising:

a graphics processor; and

a system memory controller coupled to the graphics processor, the system memory controller controlling the system memory.

2. The controller of claim 1 further comprising a cache controller for controlling a cache in the computer graphics system, the cache controller coupled to the graphics processor.

3. The controller of claim 1 further comprising a bus bridge for controlling transfer of at least some of the information on a bus in the computer graphics system, the bus bridge coupled to the graphics processor.

4. The controller of claim 1 further comprising a video processor coupled to the graphics processor.

5. The controller of claim 1 further comprising an audio processor coupled to the graphics processor.

6. The controller of claims 1, wherein the computer graphics system includes a host bus and wherein the controller is connected to the host bus.

7. An integrated controller for use in a computer graphics system having a system memory, a cache, and a first bus, the controller comprising:

a graphics controller, the graphics controller generating graphics information and controlling the system memory;

a combined bus bridge and cache controller, the combined bus bridge and system memory controller controlling the bus and the cache; and

a second bus coupling the graphics controller and the combined bus bridge and cache controller.

8. The integrated controller of claim 7, wherein the graphics controller includes a graphics processor.

9. The integrated controller of claim 7, wherein the graphics controller includes a system memory controller.

10. A graphics display system comprising:

a central processor;

a memory device;

a first controller coupled to the central processor and the memory device, the first controller having a graphics processor for generating graphics information, a memory controller for controlling the memory device, and an input and an output for receiving data from the central processor and for sending data to the central processor; and

a second controller coupled to the central processor and the first controller for receiving a command from the processor and, based on the command, controlling the flow of data between the processor and the first controller.

11. The apparatus of claim 10, wherein the graphics display system has a first bus coupled to the second controller and a second bus coupled to the second controller and wherein the second controller includes a bus bridge for conditioning information for travel between the first bus and the second bus.

12. The apparatus of claim 11, wherein the graphics display system further comprises a second memory device and wherein the second controller further includes a memory controller coupled to the bus bridge, for controlling the second memory device.

13. A graphics display system comprising:

a central processor;

a memory device for storing graphics data and non-graphics data; and

a controller coupled to the central processor and the memory device and including:

a graphics processor for generating graphics data;

a memory controller coupled to the graphics processor, for controlling the memory device; and

a plurality of data buffers coupled to the memory controller for storing data traveling between the memory device and a remainder of the graphics display system.

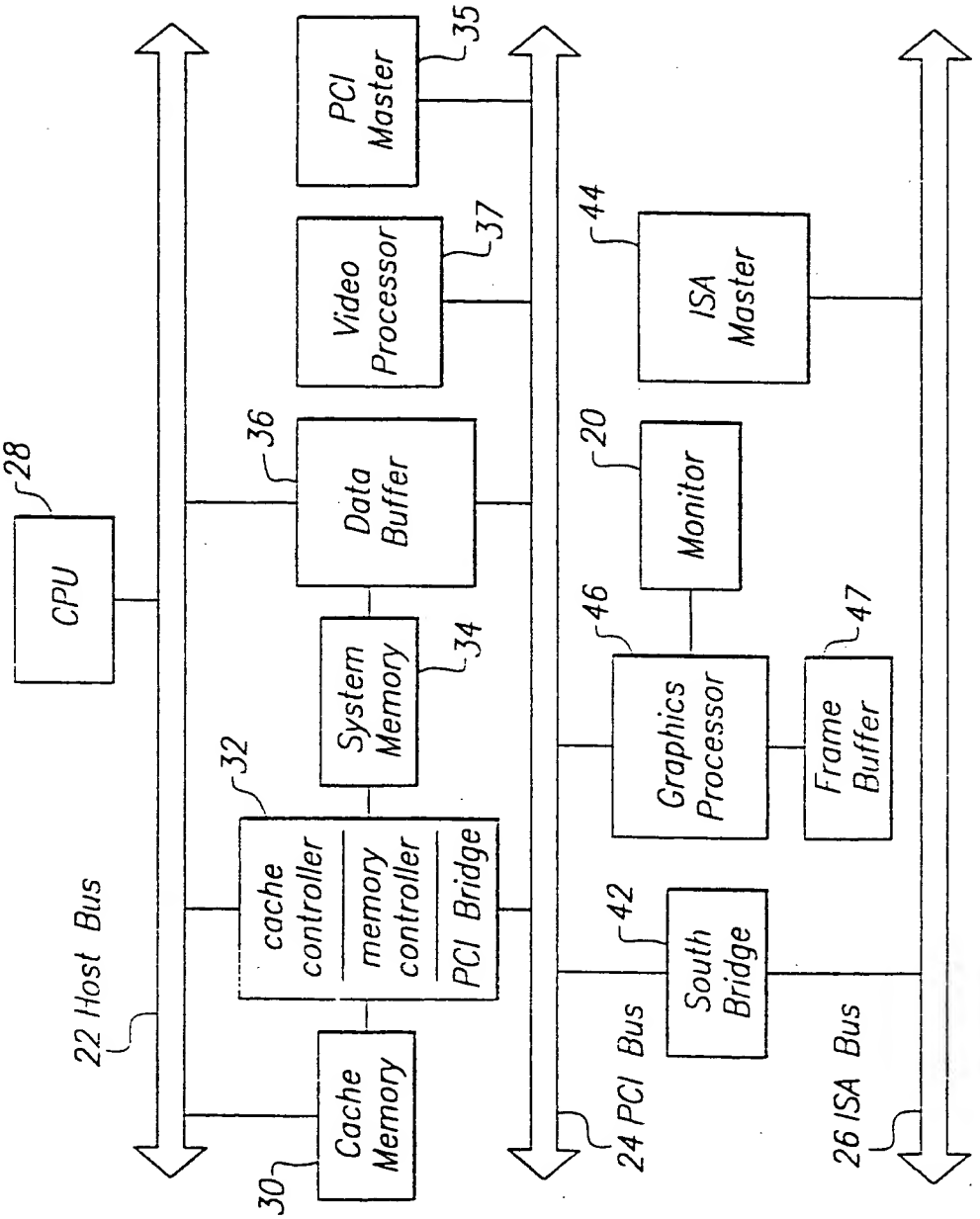


FIG. 1 (PRIOR ART)

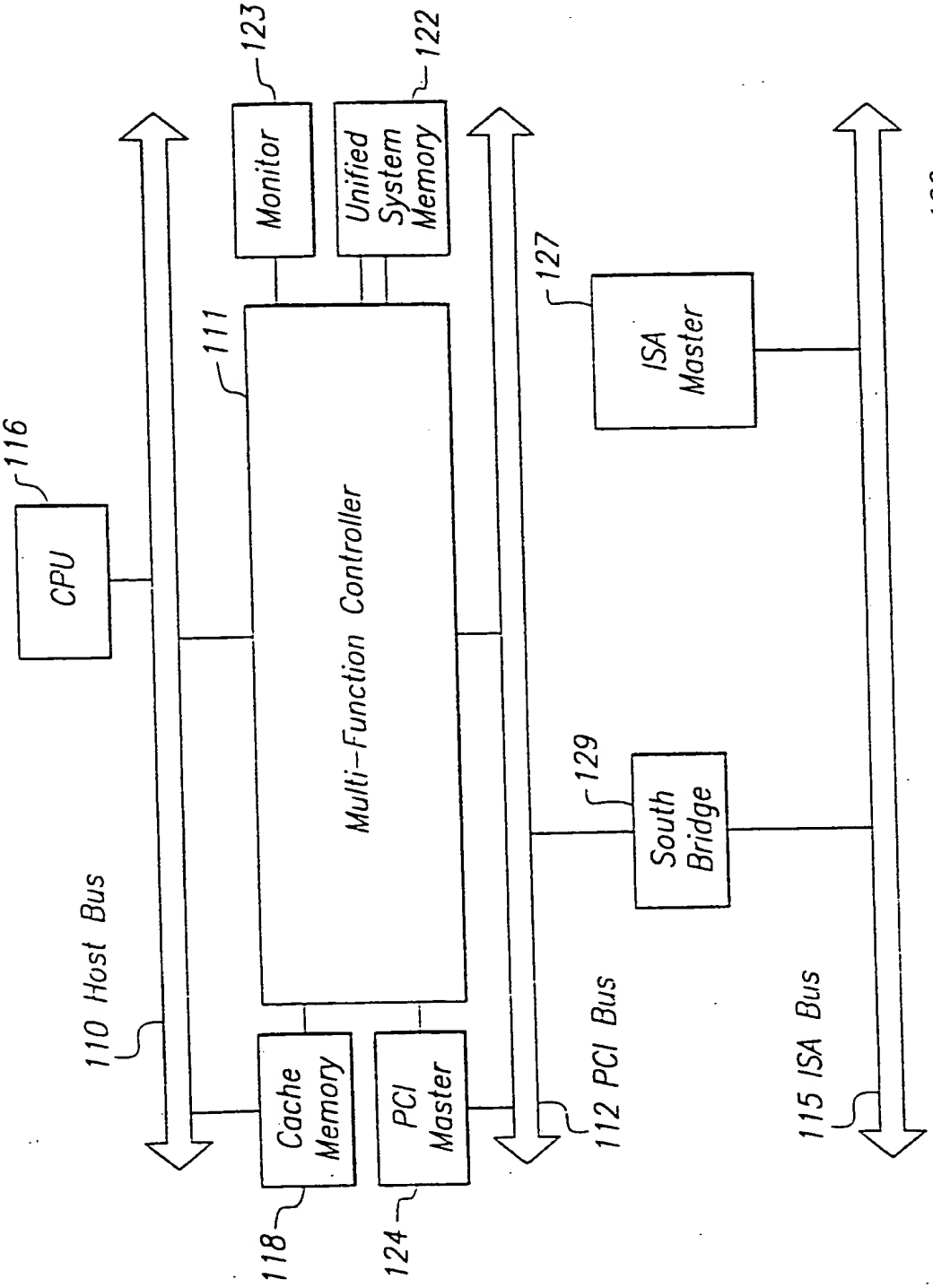

100
CPU
116
Multi-Function Controller
111
Monitor
123
Unified System Memory
122
ISA Master
127
South Bridge
129
Cache Memory
118
PCI Master
124
110 Host Bus
112 PCI Bus
115 ISA Bus

FIG. 2

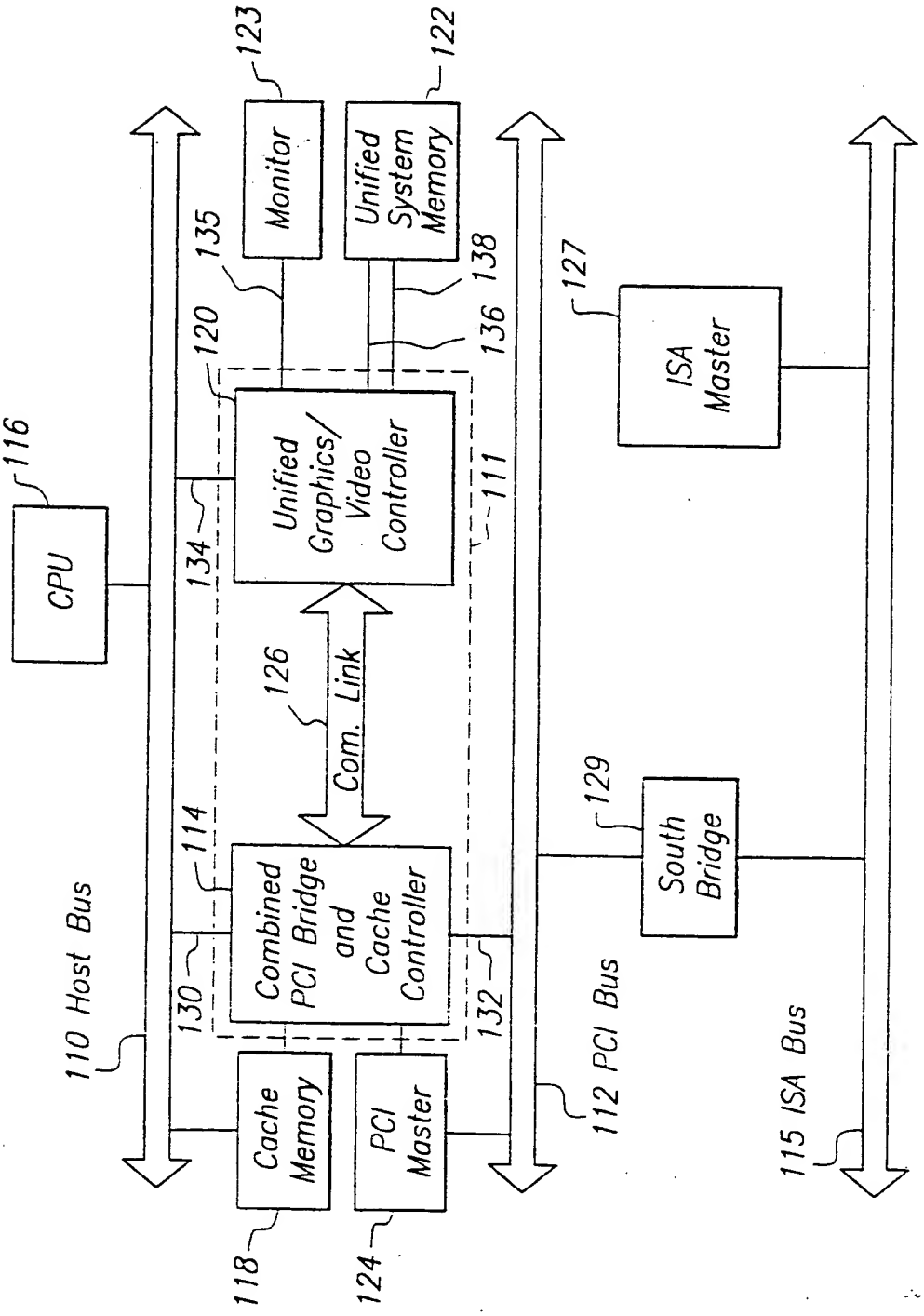

CPU
116
110 Host Bus
Cache Memory
118
PCI Master
124
Combined PCI Bridge and Cache Controller
114
130
132
Com. Link
126
Unified Graphics/ Video Controller
134
111
120
Monitor
123
135
Unified System Memory
122
138
136
ISA Master
127
South Bridge
129
112 PCI Bus
115 ISA Bus

FIG. 3

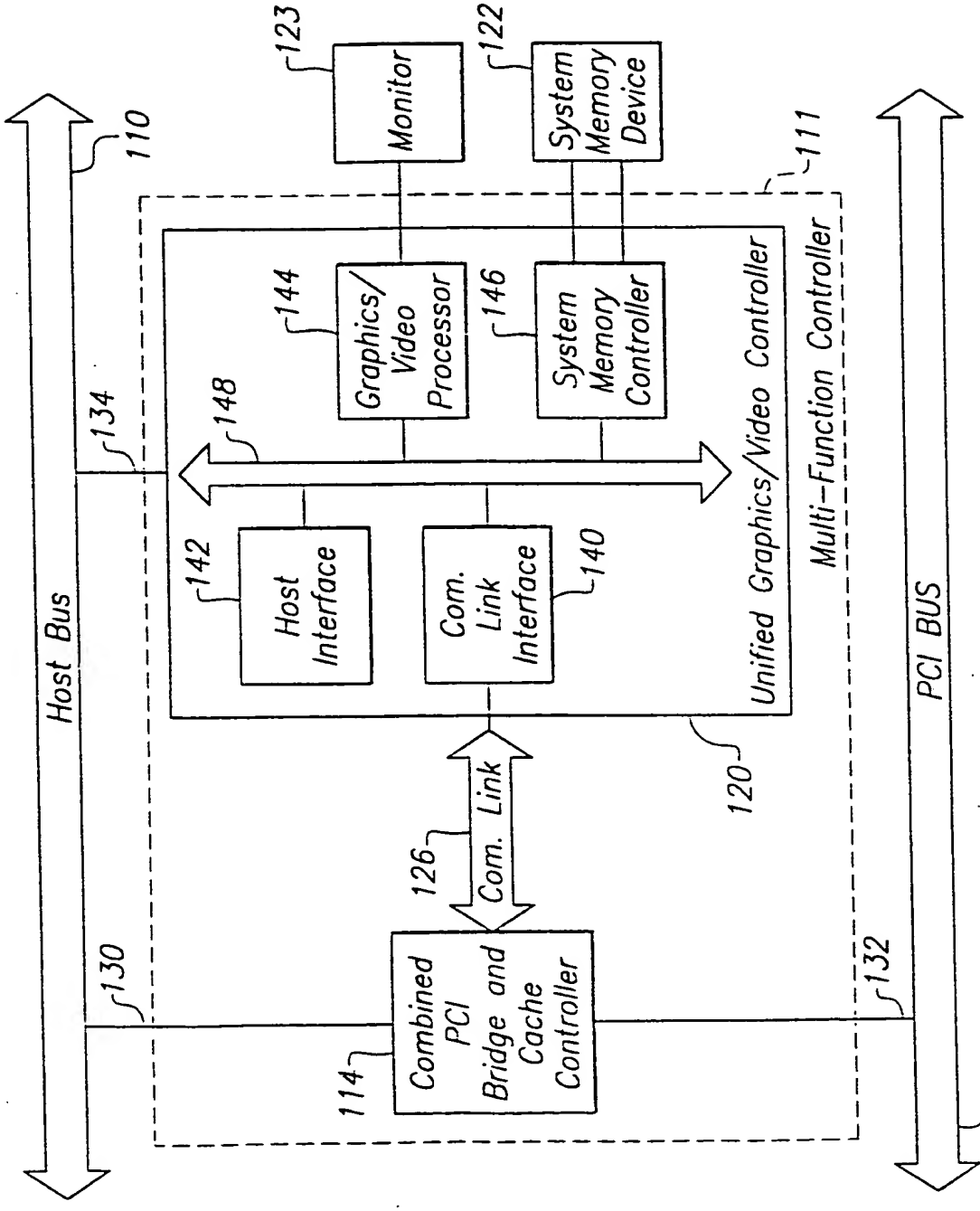
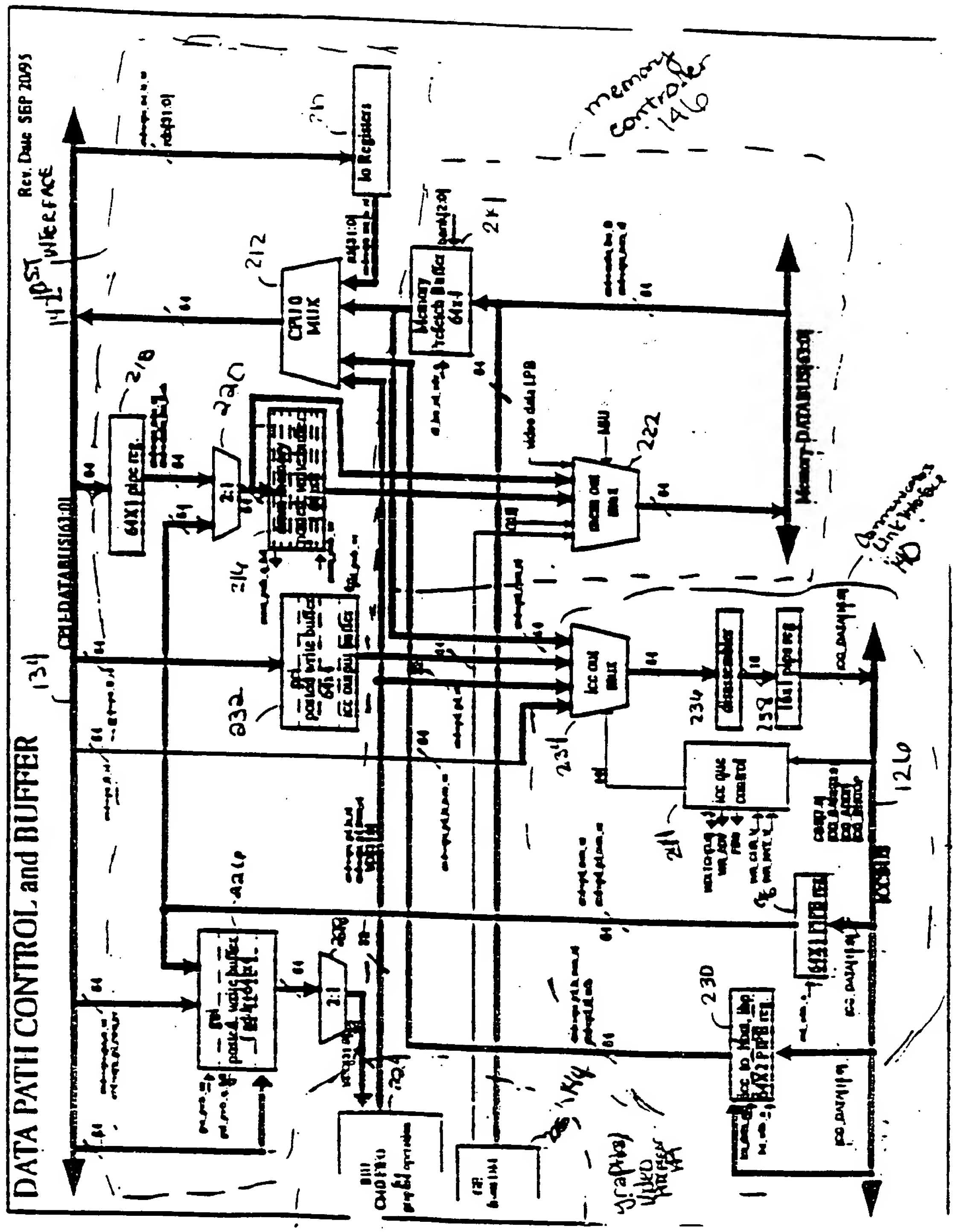

Host Bus
110
Monitor
123
System Memory Device
122
111
Multi-Function Controller
Unified Graphics/Video Controller
Graphics/ Video Processor
144
System Memory Controller
146
148
134
Host Interface
142
Com. Link Interface
140
120
Com. Link
126
130
Combined PCI Bridge and Cache Controller
114
132
PCI BUS
112

FIG. 4


DATA PATH CONTROL and BUFFER
CPU-DATABUS[63:0]
Memory-DATABUS[63:0]
CPU0 MUX
Io Registers
memory controller 146

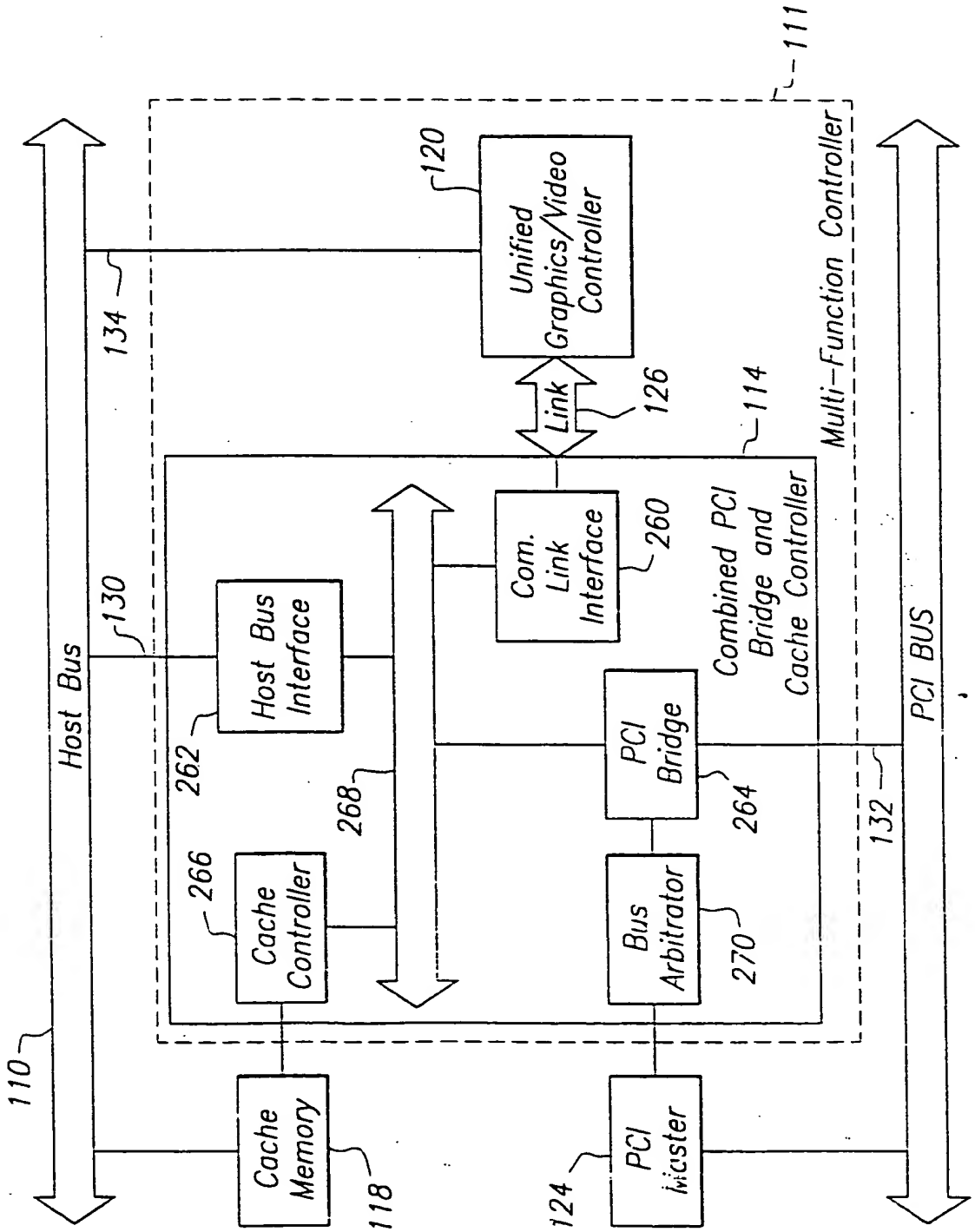

111
Multi-Function Controller
120
Unified Graphics/Video Controller
134
126
Link
114
Combined PCI Bridge and Cache Controller
Com. Link Interface
260
Host Bus
130
Host Bus Interface
262
268
PCI Bridge
264
PCI BUS
132
266
Cache Controller
Bus Arbitrator
270
110
Cache Memory
118
124
PCI Master

FIG. 6

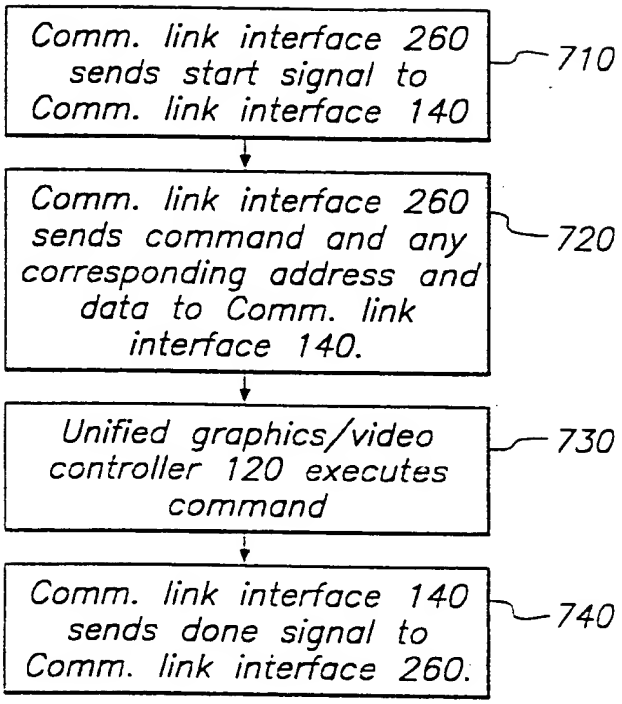

Comm. link interface 260 sends start signal to Comm. link interface 140
710
Comm. link interface 260 sends command and any corresponding address and data to Comm. link interface 140.
720
Unified graphics/video controller 120 executes command
730
Comm. link interface 140 sends done signal to Comm. link interface 260.
740

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/13356

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 13/16
US CL : 345/521
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/521, 502, 512, 302, 520, 507-509, 519, 513; 395/280, 306-308.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS; bus bridge; graphic(w)(control? or process?) or multimedia; memory control?; cache control?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P	US 5,748,203 A (TANG ET AL) 05 MAY 1998, FIGURE 2.	1, 3, 4, 6 2, 5, 7-13
Y	US 5,379,384 A (SOLOMON) 03 JANUARY 1995, FIGURE 2.	2, 7-9
Y, P	US 5732,224 A (GULICK ET AL) 24 MARCH 1998, FIGURES 1 AND 3.	4, 5
Y	US 5,553,220 (KEENE) 03 SEPTEMBER 1996 FIGURE 2.	4, 5; 7-13
Y, P	US 5,678,009 (BAINS ET AL.) 14 OCTOBER 1997 FIGURE 2.	7-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

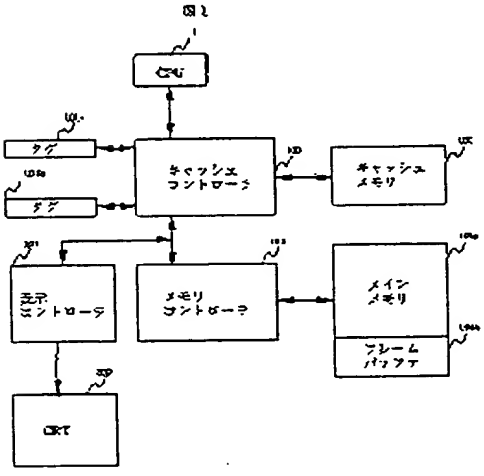
Date of the actual completion of the international search 18 SEPTEMBER 1998	Date of mailing of the international search report 15 OCT 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer KEE M. TUNG Telephone No. (703) 305-9660

Form PCT/ISA/210 (second sheet)(July 1992)*

-2- (WPAT) ;
AN - 97-421801/39
XRPX- N97-351294
TI - Display control system for data processor e.g. personal computer - uses two tags in hit evaluation of CPU access to cache memory which temporarily stores data of main memory, and hit evaluation of display data access of CRT that displays data received by display controller
DC - P85 T01
PA - (HITA) HITACHI LTD
PR - 96.01.11 96JP-002859
NUM - 1 patent(s) 1 country(s)
PN -- JP09190169 A 97.07.22 * (9739) 8p G09G-005/00
AP -- 96JP-002859 96.01.11
IC1 - G09G-005/00
IC2 - G06F-003/153 G06F-012/08
AB - JP09190169 A
The system has a cache memory (102) which temporarily stores data of a main memory (104a). A cache controller (100) determines whether the data of the main memory exists in the cache memory when memory access from a CPU (1) is generated. The cache controller uses two tags (101a,101b) in hit evaluation. The tag store the address of the data temporarily stored in the cache memory. A memory controller (103) regulates the input-output of the data from main memory.

A display controller receives and accesses display data required for display scanning. A CRT (200) displays the display data received by the display controller. **The display data are read out from the cache memory when stored in it. The display data data are read from the main memory when not stored in the cache memory**. The two tags are used in the hit evaluation of CPU access and in the hit evaluation of the display data access.

ADVANTAGE - Improves operation rate of CPU since CPU capacity reduction is prevented and influence of cache bandwidth to it is reduced. (Dwg.1/5)
FN - WPH91GP1.GIF



-1- (WPAT) .
AN - 98-302017/27
XR - 98-485593
XRPX- N98-236593
TI - Memory integrated highspeed graphics display device - assigns suitable bit for accessing cache system of CPU by graphics processor which then forwards accessed data to graphics memory
DC - P85 T01
PA - (HITA) HITACHI LTD
PR - 96.09.30 96JP-258725 97.01.28 97JP-013732
NUM - 2 patent(s) 2 country(s)
PN -- JP10105154 A 98.04.24 * (9827) 14p G09G-005/36
- KR98025110 A 98.07.06 (9927) G06F-013/12
AP -- 96JP-258725 96.09.30
- 97KR-049589 97.09.29
IC1 - G06F-013/12 G09G-005/36
IC2 - G06F-003/153 G06T-011/00 G09G-005/18
AB - JP10105154 A
The display device includes a common graphics memory (40). A CPU (10) and a graphics processor (20) are provided which access the common graphics memory. In the graphics memory, the patterning procedure information such as variety, vertex parameter to be displayed are stored.

A bit is provided which enables accessing of cache system of CPU by the graphics processor. Based on the bits, the maximum display access time is changed. The graphics processor then forwards the accessed data to the graphics memory.

ADVANTAGE - Improves accessing efficiency of graphics memory and quality of moving image. (Dwg.1/10)
FN - WPI6H1D1.GIF

図 1